CS554 Project Ideas

GeMTC:MIC – Supporting MTC Applications on Intel Xeon Phi Many-Core Accelerators

Overview

GeMTC is a CUDA based GPU framework which allows Many-Task Computing workloads to run efficiently on NVIDIA GPUs. NVIDIA is only one manufacturer of hardware accelerators; several other brands/manufacturers include AMD GPUs and the Intel Xeon Phi.

This project aims to provide support for the Intel Xeon Phi. The Intel Xeon Phi is a hardware coprocessor from Intel. It is a PCI device with roughly 60 cores and over 240 hardware threads. To program GPUs you typically need to learn another programming language such as CUDA (NVIDIA) or OpenCL (AMD). However, the Intel Xeon Phi contains traditional x86 cores, which are programmed using traditional programming languages(C, OpenMP, Pthreads.)

For this project you will write a C module that plugs into the GeMTC framework enabling tasks called from the GeMTC API to run on the Intel Xeon Phi. You will also be responsible for writing several test applications that utilize this software stack as well as some high level tests other developers can run to assert code is functioning properly.

Relevant Systems and Reading Material

GeMTC – <u>http://datasys.cs.iit.edu/projects/GeMTC</u>

Xeon Phi - <u>http://software.intel.com/en-us/mic-developer</u>

Swift - http://swift-lang.org

Preferred/Required Skills

No GPU programming skills required!

Preferred: OpenMP, Threaded programming. Required: C



Project Mentor

I am a 3rd year Ph.D. student and 2013 Starr/Fieldhouse Research Fellow from the Department of Computer Science at the Illinois Institute of Technology. I work as a Research Assistant in the Data-Intensive Distributed Systems Laboratory, a Teaching Assistant for the Department of Computer Science, and a Guest Graduate Student Researcher at Argonne National Laboratory.

Systems Laborato

I am involved in the GeMTC project, which aims to provide improved programmability and efficiency of hardware accelerators (GPGPUs, Intel Xeon Phi) in the Distributed Systems and High-Performance Computing spaces.

More information can be found at http://datasys.cs.iit.edu/~skrieder and http://datasys.cs.iit.edu



