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Memory Access Cycle and the Measurement of Memory Systems

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Memory Access Cycle and the Measurement of Memory Systems

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ABSTRACT

Due to the infamous “memory wall” problem and a drastic increase in the number of data intensive applications, memory instead of processor has become the leading performance bottleneck of modern computing systems. Evaluating and understanding memory system performance is increasingly the core of high-end computing. Conventional memory metrics, such as miss ratio, average miss latency, average memory access time, et. al., are designed to measure a given memory performance parameter, and do not reflect the overall performance of a memory system. On the other hand, widely used system measurement metrics, such as IPC, and Flops are designed to measure CPU performance, and do not directly reflect memory performance. In this paper, we proposed a novel memory metric, Access Per Cycle (APC), to measure overall memory performance with consideration the complexity of modern memory systems. A unique contribution of APC is its separation of memory evaluation from CPU evaluation; therefore, provides a quantitative measurement of the “data-intensiveness” of an application. The concept of APC is introduced; a constructive investigation of counting the number of data accesses and access cycles at differing levels of the memory hierarchy is conducted; some important usages of APC are presented. Simulation results show that APC is significantly more appropriate than existing memory metrics in evaluating modern memory systems.

Categories and Subject Descriptors

C.4 [Performance of Systems]: *design studies, measurement techniques, performance attributes.*

General Terms

Measurement, Performance

Keywords

Memory performance measurement; memory metric; measurement methodology