October 16, 1995

# cs470 - Computer Architecture 1
**Fall 1995**

## Midterm Exam
open books, open notes

Starts: **8:20 am**
Ends**: 10:00 am**

Name:____________________________________(please print)
ID:________________________

| | | |
|---|---|---|
| 1.a | 10 points | __ |
| 1.b | 5 points | __ |
| 2.a | 10 points | __ |
| 2.b | 10 points | __ |
| 3.a | 10 points | __ |
| 3.b | 10 points | __ |
| 4.a | 5 points | __ |
| 4.b | 10 points | __ |
| | **Total** | __ / 70 |

*Please return this page with your exam.*

**1.** You know the following about the *time distribution* of instructions in your favorite application (which may be a word processor, a spreadsheet or maybe a database):

| | $t_i$ | $CPI_i$ |
|---|---|---|
| ALU | 50% | 4 |
| Load/store | 40% | 6 |
| Branches | 10% | 5 |

a) compute the average CPI for your application;
b) compute the MIPS for your machine using the above table; the clock rate for your machine is 200 MHz. You get full credit for this (even if you did not solve part a if you make reasonable assumptions about the data you need.

**2.** Assume you have to write MIPS assembly code for the following piece of a C program:

```
x[5] = x[6] + a;
```

You shall assume that `a` corresponds to register $t1 and the array of words `x` begins at address $(268500976)_{10}$. You must use the native MIPS instruction set.
a) show the code;
b) what is the sequence of addresses the CPU issues to execute this code? You may assume that the first instruction to execute is at address 0x400018.

**3.** You have decided to upgrade your computer's hardware with a new disk and controller. This new disk makes every disk access two times faster. With the new disk in use disk accesses account for 20% of the running time.
a) what is the overall speedup?
b) what is the overall speedup if you also improve the graphics system with a new graphics card? The new card will make all graphics 20 times faster. Graphics represent 30% of the workload of the original machine (before any improvment is done).

**4.** You have a register-register architecture that has two addressing modes, base-displacement and memory indirect, besides register and immediate. You want to improve this architecture by eliminating the memory indirect addressing mode: this will decrease the clock cycle by 10% but will increase somehow the instruction count because you will have to replace instructions like:

```
lw   R1, @(R2)
```

with a sequence of instructions. Assume that the frequency of memory indirect addressing is 5%, and that the overall CPI does not change.

a) show the sequence of instructions that will replace every memory indirect addressing;
b) how does the performance of the new architecture compare with the performance of the original?