December 12, 1995

cs470 - Computer Architecture 1
Fall 1995

Final Exam - 1
open books, open notes

Starts: **9:00 am**
Ends**: 11:00 am**

Name:____________________________________(please print)
ID:________________________

Please indicate what is the grade you think best reflects your activity in this class:

Problem			
1	5 points	__	
2	30 points	__	(15+15)
3	25 points	__	(10+5+5+5)
4	10 points	__	
	Total	__ / 70	

Please return this page with your exam.

1. Show the memory layout of an array declared as

```
int ar[2][3][4];
```

assuming that the elements of the array are stored in column-major order.

2. Consider three machines with different cache organizations:

Cache 1: Direct mapped with one-word blocks T_{ck}=10ns
Cache 2: Direct mapped with four-word blocks T_{ck}=10ns
Cache 3: 2-way set associative with four-word blocks T_{ck}=12ns

The following measurements have been made:

Cache 1: Instruction miss rate is 4%; data miss rate 8%.
Cache 2: Instruction miss rate is 2%; data miss rate 5%.
Cache 3: Instructions miss rate is 2%; data miss rate 4%.

The same program runs on each machine. One half of the instructions contain a data reference. Assume that the cache miss penalty is `10+block_size_in_words`. The CPI for this workload, on a machine with no misses, would be 3.0.
a) determine which machine spends the most cycles in cache misses.
b) by how much is the ideal machine (T_{ck}=10ns) faster than each of the versions with cache?

3. In this problem you will use the Instruction Set you've designed in your project. Assume the following skeleton of code:

```
          .data 0xffe
inport:   .reserve 1     # reserve a 4-bit word
outport:  .reserve 1

          .text 100
myprog:   .........      # insert here your program
```

Starting with label `myprog` you will write a program that gets data from `inport` and sends the incremented data to `outport`. You should not be concerned with any communication matter. Overflows are ignored in case they occur: you just send to `outport` what's left in the destination register after you increment data. For each instruction you will indicate the address in memory where it starts, the size (in **bytes**), and the number of memory accesses necessary to complete. Use the attached lined sheet.

4. In a memory hierarchy that includes a TLB and a cache (and the main memory of course), a memory reference may encounter three different types of misses: a TLB miss, a page fault and a cache miss. Consider all the combinations of these misses (with one or more occurring). For each possibility indicate whether the event can actually occur and in what circumstances.
