March 4, 2002

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cs470 - Computer Architecture 1

Spring 2002

Midterm Exam

open books, open notes

Starts: **6:25 pm** Ends**: 8:05 pm**

Name:_____(please print)

ID:_____

Problem	Max points	Your mark	Comments
1	25		10+10+5
2	25		10+10+5
3	10		10
4	15		5+5+5
	75		

1. Your first job as a new employee with ACME Computing is to upgrade your CEO's computer with a new disk and a new disk controller. These changes will make every disk access two times faster. **With these enhancements in place**, disk accesses account for 25% of the running time. The overall cost of the system increases by 10%.

a) what is the overall speed-up?

b) what is the overall speed-up if you also improve the graphics system with a new graphics card (both enhancements at the same time)? The new card will make all graphics 15 times faster. Graphics represent 20% of the workload of the original machine (before any improvement is done).

c) Assuming just the disk improvement, decide whether the new system will be more cost effective than the current one. We say that one system is more *cost effective* than another if the ratio of performance divided by cost is higher.

2. Consider the following C statement:

```
a = a*b + c;
```

You have an 8-bit stack machine with 16 bit addresses. `a`, `b`, and `c` are of type `very short int` (i.e. 8-bit) and are stored in memory starting with the address `0x0DDD` (where DDD stands for the three left-most digits of your SSN/student_id). Their initial values are `0x2b` for `a`, `0x02` for `b`, and `0x03` for `c`. The code starts in memory at address `0x7ffc`. Below is a list of opcodes (each opcode is one byte wide):

Instruction	Opcode
`add`	`0x20`
`sub`	`0x21`
`mul`	`0x22`
`div`	`0x23`
`push`	`0x24`
`pop`	`0x25`

a) Compile the C code for this stack machine; for each instruction in the program show the instruction format; clearly mark the boundaries of each instruction.and the number of

bytes needed

Instruction	Instruction Format						

b) Show the sequence of addresses issued by the CPU to execute this code; for each address indicate whether it's a memory read or write and what's on the data bus for that particular memory access.

Address	R/W	Data	Comments

Address	R/W	Data	Comments

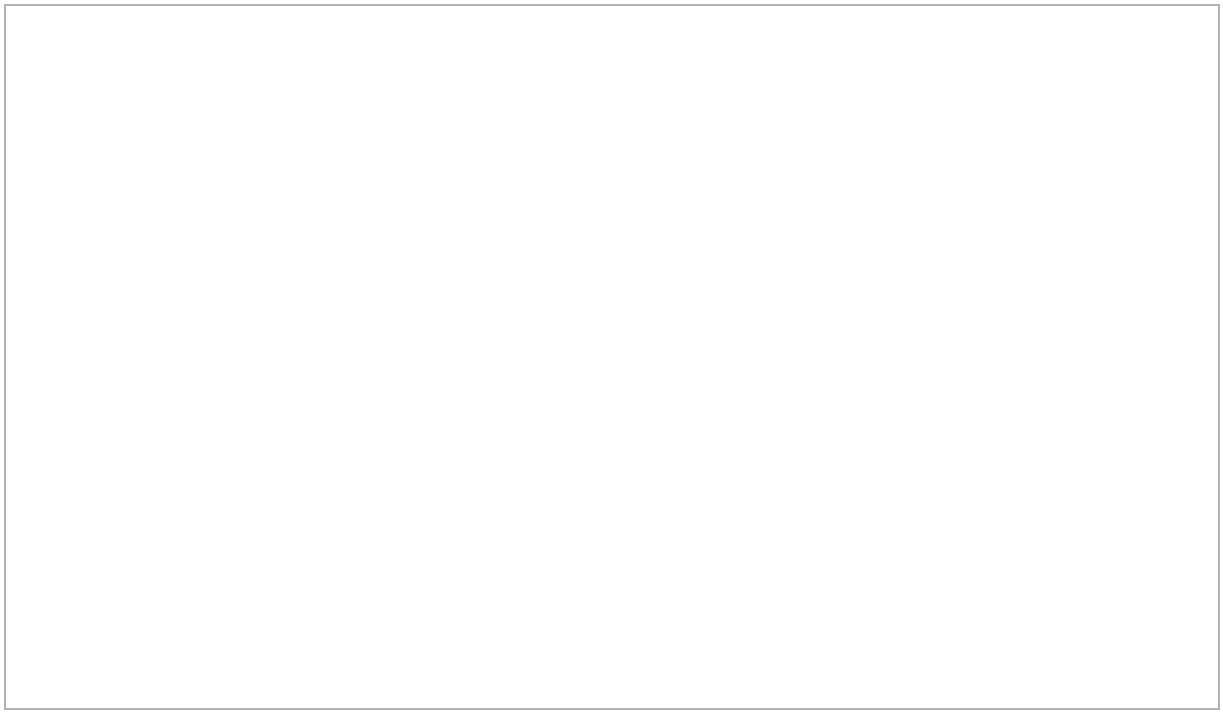
c) What is the average number of memory accesses per instruction?

3. Write MIPS assembly code for the following piece of a C program:

```
x[6] = x[5] + a;
```

You shall assume that `a` corresponds to register `$t1` and the array of words `x` begins at

address `0x10010010`. You must use the **native** MIPS instruction set.



4. We are interested in two implementations of a machine, one with and one without special floating-point hardware. Consider a program *P* with the following mix of operations

Operation	Frequency
floating-point multiply	10%
floating-point add	15%
floating-point divide	5%
integer instructions	70%

Machine *MFP* (Machine with Floating Point) has floating-point hardware and can therefore implement the floating-point operations directly. It requires the following number of clock cycles for each instruction class:

Operation	CPI
floating-point multiply	6
floating-point add	4
floating-point divide	20
integer instructions	2

Machine *MNFP* (Machine with No Floating Point) has no floating-point hardware and so it must emulate the floating-point operations using integer instructions. The integer

instructions all take two (2) clock cycles. The number of integer instructions needed to implement floating-point operations is as follows:

Operation	Integer Instructions Count
floating-point multiply	30
floating-point add	20
floating-point divide	50

Both machines have a clock-rate of 1 GHz.

a) Find the MIPS ratings for each machine

b) If machine *MFP* needs 500 million instructions to execute program *P*, how many inte-

ger instructions does *MNFP* need for the same program?

c) Assuming the instruction counts in (b) above, what is the execution time (in seconds) for *P* for both *MFP* and *MNFP*?