March 4, 1996

cs470 - Computer Architecture 1
Spring 1996

Midterm Exam

Name:_____ (please print)
ID:_____

1.a	10 points	___
1.b	10 points	___
1.c	10 points	___
1.d	10 points	___
2.a	10 points	___
2.b	20 points	___
3	10 points	___
4.a	10 points	___
4.b	10 points	___
	Total	___ / 100

Please return this page with your exam

1. We are interested in two implementations of a machine, one with and one without special floating point hardware. Consider a program P, with the following mix of operations:

floating point add	15%
floating point multiply	10%
floating point divide	5%
integer instructions	70%

Machine **MFP** (Machine with Floating Point) has floating-point hardware and can therefore implement the floating point operations directly. It requires the following number of clock cycles for each instruction class:

floating point add	4
floating point multiply	6
floating point divide	20
integer instructions	2

Machine **MNFP** (Machine with No Floating Point) has no floating point hardware: therefore it must emulate the floating point operations using integer instructions. The integer instructions all take 2 clock cycles. The number of integer instructions needed to implement each of the floating point operations is as follows:

floating point add	20
floating point multiply	30
floating point divide	50

Both machines have a clock rate of 100 MHz.

a) find the native MIPS ratings for the two machines.
b) if machine MFP needs 300,000,000 instructions for program P, how many integer instructions does the machine MNFP require for the same program?
c) assuming the instruction counts above, what is the execution time (in seconds) for program P on the two machines?
d) Assuming that each floating point operation counts as 1, and that MFP executes 300,000,000 instructions, find the MFLOPS rating for the two machines.

2. Write MIPS assembly code (native) to implement the following C statement:

```
x[5] = y[6] + z;
```

You shall assume that the variable `z` of size word corresponds to register `$t0`, and that the arrays `x[]` and `y[]` begin in memory at addresses `0x10000000` and `0x10000100` respectively. Also assume that the initial value of `z` is `0x55` and that the initial values in `y[]` are the addresses at which they are stored (i.e. `y[0] = 0x10000100`, etc.).

a) show your code;

b) show what is the sequence of addresses the CPU issues to execute this piece of code; also show what the CPU reads/writes from/to memory for each address it issues. You may assume that the first instruction to execute is at address `0x400018`. For this part use the ruled page attached to your exam.

3. You have decided to upgrade your machine: you consider adding a floating-point unit that speeds up every floating-point operation 10 times, and a new disk system that will make every disk access two times faster than it is now. You know that your favorite application, running on the current machine, spends 20% of the time executing floating-point operations. After you enhance your machine with both the floating-point unit and the new disk , disk accesses account for 40% of the time.

What is the overall speedup?

4. You have a 2-address, register-register architecture which has two addressing modes, base-displacement and absolute (besides register and immediate). You try to improve this architecture by eliminating the memory absolute addressing mode: as a result the clock rate will increase by 10%. Also as a result the instruction count will increase as you'll have to replace instructions like:

```
lw    R1, (1000)
```

with a sequence of instructions. Assume that the frequency of memory direct addressing is 15% and that the overall CPI does not change.

a) show the sequence of instructions that will replace every memory absolute addressing;

b) how does the performance of the new architecture compare with the performance of the original?

Address	Operation (R/W)	Comment