V2

May 6, 1996

cs470 - Computer Architecture 1
Spring 1996

Final Exam
open books, open notes

Starts: **6:20 pm** Ends**: 8:00 pm**

Name:_______________________________________(please print)

ID:__________________________

Problem	Max points	Your mark	Comments
1	10		10
2	60		10+10+10+5+5+5+5+10
3	30		10*3
	100		

What happens with this paper (mark one): **Discard**

Mail at the following address:

1. A CPU running at 100 MHz receives interrupts from a timer every 1 milliseconds. The interrupt handler spends 80 instructions to handle such an interrupt. What is the CPI for the application if the effect of interrupts is taken into account? You may assume that the CPI of the application running on the machine without interrupts is 1.5

2. Assume the following piece of MIPS assembly:

```
       .data 0x10000000
var1: .word 0x8192a3b4
var2: .word 0

       .text 0x400020
main: subu  $sp, $sp, 4
       sw    $ra,  0($sp)
       jal   Mistery
       lw    $ra, 4($sp)
       addu  $sp, $sp, 4
       jr    $ra

       .text 0x401100
Mistery:
       lui   $t0, 4096
       lb    $t1, X($t0)        # X is the first digit of your SSN modulo 4
       sw    $t1, 4($t0)
       jr $ra
```

a) Show the sequence of addresses issued by the CPU to execute this code. You may assume that the initial value of the stack pointer is `0x7ffffff0`.

Address (in hexadecimal)	Cache Hit or Miss	TLB Hit or Miss	Page Faults

b) Assume a direct mapped cache with a size of 32 bytes, with 8 bytes per block and a write-through policy. Assume that all the blocks in the cache are invalid at the time the program starts executing. Show the contents of the cache after the last statement has been executed. Make sure to label each reference as a hit or miss in the 'Cache Hit or Miss' column of the table. Use the ruled page attached to this exam to show the cache. Clearly mark the limits of your cache and label the fields of it.

c) What is the miss-rate?

d) The system on which you run the program has virtual memory, with a page size of 4KB and a main memory of 16MB. Show the size of various fields in the virtual address.

e) What is the size of the page table? Assume that each entry in the table has a size which is a multiple of byte; each entry uses four bits for various purposes (‘Valid’, ‘Dirty’, etc.).

f) Assume that initially the operating system brings in the main memory only a page, the one which contains the code to execute (starting with the label ‘main’). In the column ‘Page faults’ of the table above, indicate which references will generate a page fault.

g) The system also has a fully associative TLB with two blocks. Initially all the blocks in the TLB are invalid. In the column ‘TLB Hit or Miss’ of the table above, indicate which references are TLB hits and which are misses.

h) Show the final contents of the TLB. Show the size of various fields.

i) What is the contents of the variable `var2` after the program executes?

3. On the datapath attached to this exam, fill the shaded areas with the values of the data they are pointing to during the execution of the branch in the following piece of MIPS code:

```
      .text 0x400000
      li    $8, 3
      li    $9, 4
loop: addi  $9, $9, 1
      beq   $8, $9, loop
```

No control signals are shown on the single cycle datapath and you should not be concerned with any. If a certain part of the datapath is undefined or irrelevant at the time the instruction is executed then say so in the box.
