V2

March 10, 1997

# cs470 - Computer Architecture 1

**Spring 1997**

## Midterm Exam

open books, open notes

Starts: **10:10 am** Ends**: 12:00 pm**

Name:_____(please print)

ID:_____

| Problem | Max points | Your mark | Comments |
|---|---|---|---|
| 1 | 10 | | 5+5 |
| 2 | 25 | | 20+5 |
| 3 | 20 | | 10+10 |
| 4 | 25 | | 15+5+5 |
| | 80 | | |

**1.** You know the following about the frequency of instructions in your favorite application (which may be a word processor, a spreadsheet or maybe a database):

| | $f_i$ | $CPI_i$ |
|---|---|---|
| ALU | 57% | 3 |
| Load/store | 33% | 5 |
| Control | 10% | 4 |

a) compute the average CPI for your application;

b) compute the MIPS rating for your machine using the above table; assume a clock rate of 200 MHz.

**2.** Given the following piece of MIPS assembly:

```
        .data 0x10000000
var1:   .word 0x8192a3b4
var2:   .word 0

        .text 0x400020
main:   subu  $sp, $sp, 4
        sw    $ra,  0($sp)
        jal   Mistery
        lw    $ra, 0($sp)
        addu  $sp, $sp, 4
        jr    $ra

        .text 0x400100
Mistery:
        lui   $t0, 4096
        lb    $t1, X($t0)       # X is the last digit of your SSN modulo 4
        sw    $t1, 4($t0)
        jr $ra
```



© Virgil Bistriceanu, 1997

a) Show the sequence of addresses issued by the CPU to execute this code. The initial value of the stack pointer is **`0x7fffff00`**.

| Instruction | Address (in hexadecimal) | Read/Write |
|---|---|---|
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |

b) What is the final value of **`var2`**? You assume a Big Endian memory model.



© Virgil Bistriceanu, 1997

**3.** You have decided to upgrade your computer's hardware with a new disk and controller. This new disk makes every disk access two times faster. With the new disk *in use* disk accesses account for 25% of the running time.

a) what is the overall speedup?

b) what is the overall speedup if you also improve the graphics system with a new graphics card? The new card will make all graphics 10 times faster. Graphics represent 45% of the workload of the original machine (before any improvment is done).



© Virgil Bistriceanu, 1997

**4.** You have been asked to compare the memory efficiency of two different styles of instruction sets, one for an *accumulator* architecture and the second for a two-address *memory-memory* (all operands are in the memory) architecture. The following can be assumed:

- the opcode is always one byte
- all memory addresses are 16 bit wide
- all data operands are four bytes
- all instructions are an integral number of bytes in length

There are no optimizations to reduce memory traffic, and the variables `a`, `b`, `c`, and `d` are initially in memory.

a) Write the two code sequences for the following C code:

```
a = a + c;
b = a + c;
d = a – b;
```

**Accumulator Architecture**

| Assembly Instructions | Instruction Bytes Fetched | Data Bytes Transferred |
|---|---|---|
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |

;

**Memory-Memory Architecture**

| Assembly Instructions | Instruction Bytes Fetched | Data Bytes Transferred |
|---|---|---|
| | | |
| | | |
| | | |
| | | |



© Virgil Bistriceanu, 1997

**Memory-Memory Architecture**

| Assembly Instructions | Instruction Bytes Fetched | Data Bytes Transferred |
|---|---|---|
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |

b) Which architecture is more efficient as measured by code size?

c) Which architecture is most efficient as measured by total memory bandwidth required (code + data)?



© Virgil Bistriceanu, 1997