V2

May 12, 1997

cs470 - Computer Architecture 1
Spring 1997

Final Exam
open books, open notes

Starts: **10:00 am** Ends**: 12:00 pm**

Name:_________________________________(please print)

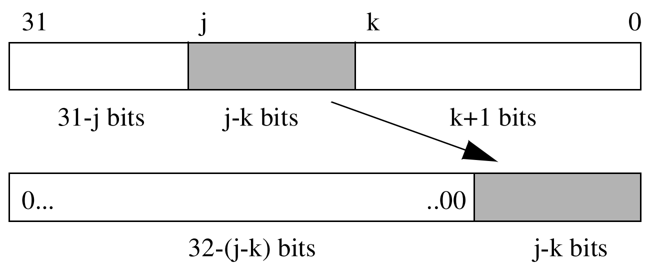
ID:______________________

Problem	Max points	Your mark	Comments
1	25		10+5+10
2	60		10+10+10+5+5+5+5+5+5
3	15		
	100		

In addition there will be up to 15 points of extra credit for the paper describing the cache configuration of some popular CPUs and 15 points extra credit for the paper that analyzes differences between unified and separate caches.

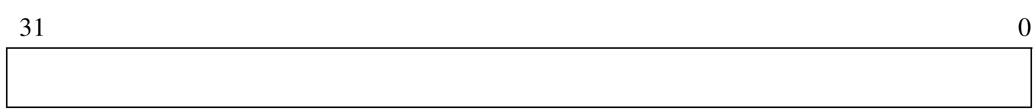
What happens with this paper (mark one):**Discard** **Mail** at the following address:

1. Some computers have explicit instructions to extract an arbitrary field from a 32-bit register and place it in the least significant bits of a register. The operation is depicted below:



a) Find the shortest sequence of MIPS native instructions that extracts a field, assuming that k=9, j=17, the field is extracted from register `$t1` and the result is stored in register `$t0`.

b) Assume that we want to introduce such an instruction in the MIPS instruction set. Indicate a possible format for this instruction.



c) What extra hardware resources would be needed to support this instruction on the single datapath MIPS (figure 5.22 at page 295)? On the last page of this exam redraw the datapath to include these extra resources.

2. Assume the following piece of MIPS assembly:

```
        .data 0x10000000
var1:   .word 0x8192a3b4
var2:   .word 0

        .text 0x400020
main:   subu  $sp, $sp, 4
        sw    $ra,  0($sp)
        jal   Misery
        lw    $ra, 0($sp)
        addu  $sp, $sp, 4
        jr    $ra

        .text 0x400100
Misery:
        lui   $t0, 4096
        lb    $t1, X($t0)       # X is the first digit of your SSN modulo 4
        sw    $t1, 4($t0)
        jr $ra
```

a) Show the sequence of addresses issued by the CPU to execute this code. You may assume that the initial value of the stack pointer is **0x7ffffe0**.

Address (in hexadecimal)	Cache Hit or Miss	TLB Hit or Miss	Page Faults

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b) Assume a direct mapped cache with a size of 32 bytes, with 4 bytes per block and a write-back policy. Assume that all the blocks in the cache are invalid at the time the program starts executing. Show the contents of the cache after the last statement has been executed. Make sure to label each reference as a hit or miss in the 'Cache Hit or Miss' column of the above table. Use the ruled page attached to this exam to show the cache. Clearly mark the limits of your cache and label the fields of it.

c) What is the miss-rate?

d) The system on which you run the program has virtual memory, with a page size of 8 KB and a main memory of 32 MB. Show the size of various fields in the virtual address.

e) What is the size of the page table? Assume that each entry in the table has a size which is a multiple of byte; each entry uses four bits for various purposes ('Valid', 'Dirty', etc.).

f) Assume that initially the operating system brings in the main memory only a page, the one which contains the code starting with the instruction labeled *main*. In the column 'Page faults' of the table above, indicate which references will generate a page fault.

g) The system also has a fully associative TLB with two blocks. Initially all the blocks in the TLB are invalid. In the column 'TLB Hit or Miss' of the table above, indicate which references are TLB hits and which are misses.

h) Show the final contents of the TLB. Show the size of various fields.

i) What is the contents of the variable **`var2`** after the program executes? Assume a Little Endian memory model.

3. Cache C1 is direct mapped with 16 one-word blocks. Cache C2 is direct mapped with 4 four-word blocks. Assume that the miss penalty for C1 is 8 clock cycles and the miss penalty for C2 is 11 clock cycles. Assuming that the caches are initially empty, find a reference string for which C2 has a lower miss rate but spends more clock cycles on cache misses than C1. Use word addresses. The reference string will start with the most significant digit of your SSN. For the reference string show the hits and misses for each cache.

Appendix
